Section 1: Administrative & Core Identity

Project Title

Development of High-Performance Standard Cell Library in Sub-Micron Technology for DSP Applications

Student Team

Sl.No.	Name	Role / Contribution
1	**Nikhil Prabhu I (Project Lead)**	Literature Survey, Simulation of all logic gates
2	Srujan M N	Simulation of logic gates, Full Adders, Various Adders using MTCMOS, Array Multiplier
3	Yashaswini Mohan	Simulation of logic gates, Full Adders, Various Adders using MTCMOS, Array Multiplier
4	Vismaya Udagatti	Simulation of logic gates, Full Adders, Various Adders using MTCMOS, Array Multiplier
5	Ankesh N	Literature Survey, Simulation of all logic gates

Academic Details

Sl.No.	Name	USN	Current Status
1	**Nikhil Prabhu I (Project Lead)**	4MC22EC069	Studying in 8th Semester
2	Srujan M N	4MC21EC099	Higher Studies
3	Yashaswini Mohan	4MC21EC113	Higher Studies
4	Vismaya Udagatti	4MC21EC110	Working in Keyence India Pvt. Ltd
5	Ankesh N	4MC22EC012	Studying in 8th Semester

Institution

University/College: Malnad College of Engineering, Hassan

Project Duration

Project Dates: February 2025 – March 2026

Key Adviser / Mentor

Poornima M R, Assistant Professor, ECE Department, MCE, Hassan

Grant Information

Grant Approved: ₹1,00,000

Section 2: Visual Assets
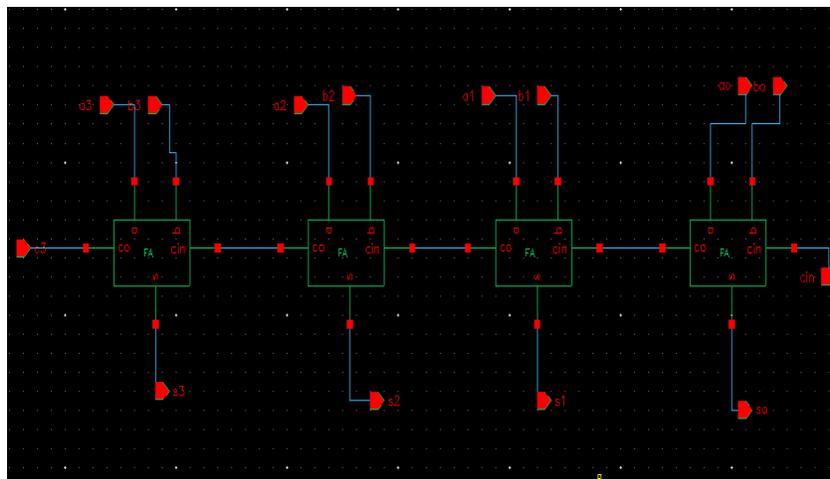
Student Profile Photos

Nikhil Prabhu I   **Srujan M N**   **Yashaswini Mohan.** **Vismaya Udagatti.**   **Ankesh N**
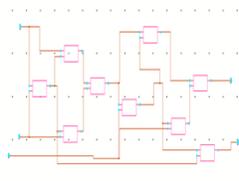
Project Images

Process Photo 1:
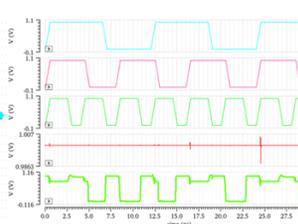

Process Photo 2:

Power and Delay analysis of 1 Bit Full Adder using NAND and Basic Gates.

Using NAND gates only
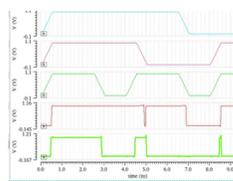
Multi Threshold Voltages	Delay (s)	Power (W)
High Threshold	2.67E-09	9.15E-07
Low Threshold	1.48E-10	1.23E-06
PMOS High	1.47E-10	1.11E-06
NMOS High	2.63E-09	1.00E-06

Using Basic gates only
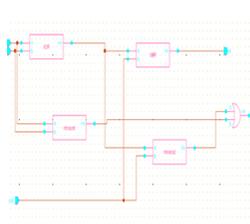
Configuration	Delay (s)	Power (W)
High Threshold	2.65E-09	9.51E-07
Low Threshold	4.60E-09	1.26E-06
PMOS High	2.64E-09	1.01E-06
NMOS High	4.59E-09	6.53E-06

Process Photo 3:

Observations: *Power, Delay, and PDP.*

Table 5 Power-Delay Product in Hybrid Adder

Method	Delay (ns)	Power (µW)	PDP (ns·µW)
Hybrid using CSA and Carry Skip Adders [32]	0.070	494	34.58
Proposed	0.195	19.1	3.7245

Table 6 Power-Delay Product in Carry Select Adder

Method	Delay (ns)	Power (µW)	PDP (ns·µW)
Proposed	0.096	82.35	7.9056
CSLA using Method 1 [35]	4062	0.0099	40.21
CSLA using Method 2 [35]	8141	0.0064	52.102

Table 7. Power-Delay Product in Brent Kung Adder

Method	Delay (ns)	Power (µW)	PDP (ns·µW)
Proposed	0.0875	7.10	0.62125
Parallel Prefix [34]	37.88	3.98	150.8224
Parallel Prefix [36]	19.39	0.9365	18.1561

Table 8 Power-Delay Product in Ripple Carry Adder

Method	Delay (ns)	Power (µW)	PDP (ns·µW)
Proposed	0.0803	5.31	0.426393
RCA using Basic CMOS [32]	0.155	235	36.425
RCA using Traditional NAND Full Adders [33]	108.1	0.0003124	0.033757
RCA using NAND-HA-FA [33]	0.3133	0.08295	0.025972

Platform / Software Configuration

The system configuration for this study includes a Red Hat Linux operating system and CADENCE Virtuoso software, optimized for performance on a machine with an Intel Core i5 processor.

Section 3: Narratives

The Hook (One-Line Summary)

> *Standard cells allow tools to automatically synthesize a circuit and optimize area, power consumption and timing. In this work, a high-performance Standard Cell Library (SCL) will be developed for DSP applications in 45nm technology using CADENCE software tool.*

Problem Statement

(The "Why" – Challenge being addressed, its significance, and who is affected)

- As the complexity of design continues to increase, full custom design is no longer feasible. Designs based on different technology at competitive cost have always been challenges to manufacturers.

- Some of the driving factors include portability, mobility, accuracy, and increased performance demands.
- This brings the manufacturers to adapt certain methods such as decreasing component sizes while simultaneously increasing performance.

The Solution

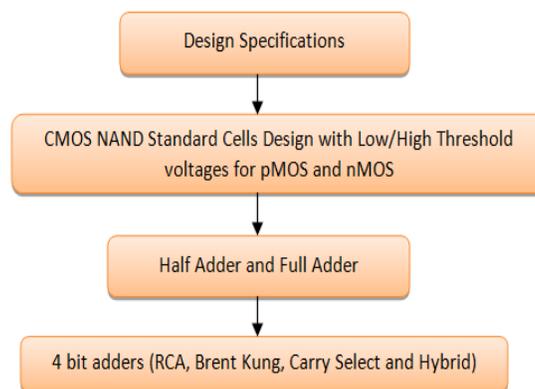(The "What" – Developed solution, product, or platform)

1. Exhaustive literature survey on available standard cell library in terms of low power, area optimization and high performance.
2. Design, development and analysis of Gates (Basic, Universal and Exclusive) and Flip Flops with different drive strength in 45nm technology.
3. Implementation of combinational circuits using high-performance standard cell library.

Methodology & Key Technology

(The "How" – Key tools, technologies, methodologies used)

The system configuration for this study includes a Red Hat Linux operating system and CADENCE Virtuoso software, optimized for performance on a machine with an Intel Core i5 processor.

Methodology Flow:

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┌─────────────────────────────┐
│    Design Specifications    │
└─────────────────────────────┘
              │
              ▼
┌───────────────────────────────────────────────┐
│ CMOS NAND Standard Cells Design with Low/High  │
│   Threshold voltages for pMOS and nMOS         │
└───────────────────────────────────────────────┘
              │
              ▼
┌─────────────────────────────┐
│   Half Adder and Full Adder │
└─────────────────────────────┘
              │
              ▼
┌───────────────────────────────────────────────────┐
│ 4 bit adders (RCA, Brent Kung, Carry Select and Hybrid) │
└───────────────────────────────────────────────────┘
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Key Findings & Results

Various adders and multipliers were compared using different methods in terms of power, delay, and power-delay product.

> **Impact:** Presented a research paper at ICDCCS, titled "Design and Comparative Analysis of Adders using MTCMOS in 45nm Technology for High Speed Applications" on 19th April 2025 at Kalpataru Institute of Technology, Tumkur, Karnataka, India.

Future Scope & Next Steps

- This project will be used for DSP applications where high-performance standard cells are required.
- Further research: Go beyond CMOS technology and use FinFET and GAA transistors to meet the technology requirements of emerging trends. However, advanced tools like CADENCE with these features are needed.